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10/726,490	12/04/2003	Zi-Ping Chen	681954-45U1	7535

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EXAMINER	
BAUER, SCOTT ALLEN	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,490	CHEN ET AL.	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04 December 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/26/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 12, 13, & 26 are objected to because of the following informalities:

2. With regard to Claim 12, the applicant refers to the SCR comprising a different p-type diffused region partially formed in the n-well to serve as a drain of the p-type resistor. Claim 12 goes on to recite that the p-type diffused region serves as a source of the p-type transistor. As written, it is unclear whether the p-type diffused region serving as the source of the p-type transistor, is the p-type diffused region of Claim 11 or Claim 12. For the purpose of this Office Action, the p-type diffused region serving as the source of the transistor is the p-type diffused region recited in Claim 11. Appropriate correction is required.

3. With regard to Claim 13, the applicant refers to the SCR comprising a different n-type diffused region formed in the p-substrate to serve as a drain of the n-type resistor. Claim 13 goes on to recite that the n-type diffused region serves as a source of the n-type transistor. As written, it is unclear whether the n-type diffused region serving as the source of the n-type transistor, is the n-type diffused region of Claim 11 or Claim 13. For the purpose of this Office Action, the n-type diffused region serving as the source of

the transistor is the n-type diffused region recited in Claim 11. Appropriate correction is required.

4. With regard to Claim 26, line 2 contains a minor spelling error. The Examiner suggests that the word "a", be changed to –and--.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-15 & 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Su et al. (US 6590261) in view of Zunino (US 4646124).

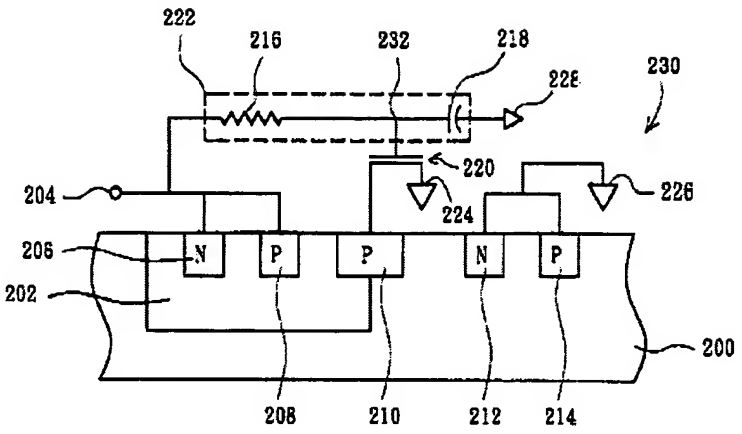
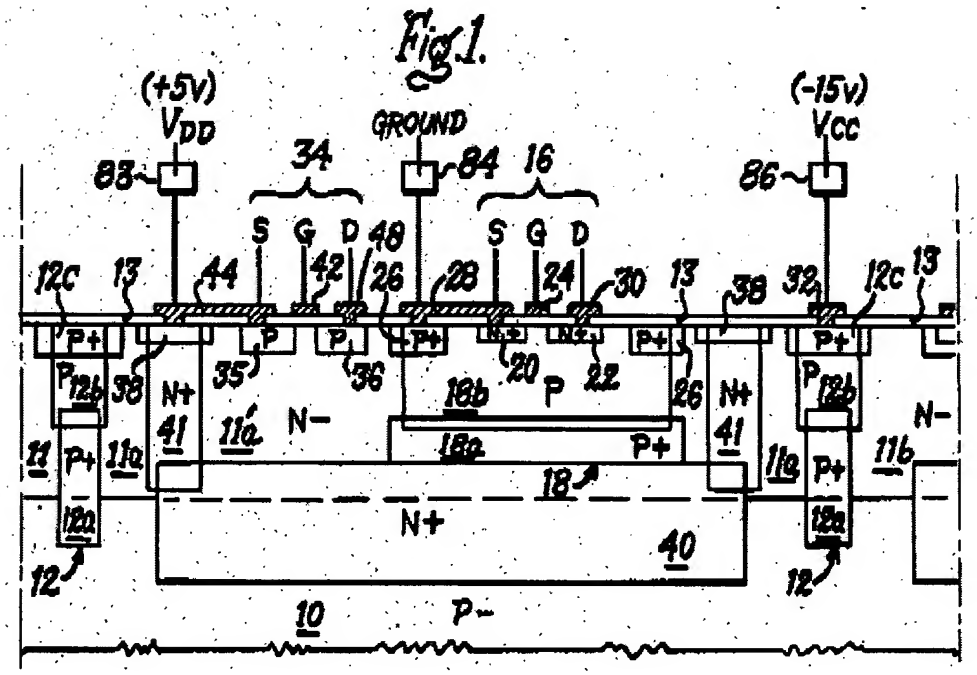


FIG. 4



7. With regard to Claim 1, Su et al., in Figure 4, teaches an electrostatic discharge protection structure comprising an SCR (230) a MOS transistor (220) and an RC control circuit (222) coupled to the gate of the MOS transistor (column 4 lines 16-18). The

control circuit is in response to a first voltage applied to the first and second gates providing a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state (column 4 lines 42-58).

Su et al. does not teach that a first transistor of a first type is integrally formed with the SCR including a first gate. Su et al. further does not teach that the MOS transistor (220) is integrally formed with the SCR including a second gate.

Zunino, in Figure 1, teaches a level-shifting BiCMOS integrated circuit. The integrated circuit forms a silicon-controlled rectifier, which Zunino refers to as a PNPN transistor (column 3 lines 59-63). A complimentary pair of MOS transistors forms the SCR (column 1 lines 65-68 and column 2 lines 1 & 2). Zunino also teaches that the level-shifting circuit is provided for the purpose of reducing the gain of the PNPN transistor enough to prevent latch-up of the circuit (column 1 lines 42-59).

Zunino teaches that the SCR comprises a first transistor (34) of a first type, integrally formed with the SCR including a first gate (42). Zunino further teaches that the SCR comprises a second transistor (16) of a second type integrally formed with the SCR including a second gate (24). This circuit is further demonstrated in figure 3 by transistors 16 and 34. The gates are tied together and form a single node.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Su et al. with Zunino by replacing the SCR (200) and the MOS transistor (220) taught by Su et al. with the PNPN transistor (Zunino Figure 1) taught by Zunino. In the ESD protection device taught by Su et al. in

view of Zunino, the anode (44) of the PNPN transistor is coupled to the positive terminal of the power source as taught by Zunino, the cathode of the PNPN transistor is coupled to the negative terminal of the power source as taught by Zunino and the two gates are coupled to the output terminal (106) as taught by Zunino. The RC control circuit as taught by Su et al. is coupled to the output terminal (106). The circuit thus eliminates the need for discrete transistor (220) as taught by Su et al. by replacing it with the second MOS transistor (16) taught by Zunino. The elimination of transistor 220 is done for the purpose of reducing the cost of the circuit as the need to purchase discrete MOS transistors is eliminated.

8. With regard to Claim 2, Su et al. in view of Zunino, teaches the circuit of Claim 1. Zunino, in Figure 3, further discloses that the first and second gates are coupled to an output terminal (106).

9. With regard to Claim 3, Su et al. in view of Zunino teaches the circuit of Claim 1. Su et al. further discloses that the control circuit comprises a resistor and a capacitor. The circuit taught by Su et al. in view of Zunino teaches that the output terminal (106) is disposed between the resistor and capacitor.

10. With regard to Claim 4, Su et al in view of Zunino teaches the circuit of Claim 1, Su et al. further discloses that the control circuit comprises an RC circuit with a resistor

(216) and a capacitor (218) which set a time constant of the circuit (column 4, lines 25 & 26).

11. With regard to Claim 5, Su et al. in view of Zunino discloses the circuit of Claim 1. Zunino, in Figure 3 further discloses that the SCR comprises a p-type substrate (18b) an n-well (11'a) formed in the p-type substrate, a p-type diffused region (35) formed in the n-well and an n-type diffused region (22) formed outside of the n-well.

12. With regard to Claim 6, Su et al. in view of Zunino teaches the circuit of Claim 5. Zunino, in Figure 3, further discloses that the first transistor (16) is an n-channel transistor (column 3 lines 8 & 9). An n-channel transistor inherently comprises a channel formed in the n-well beneath the gate region of the transistor when a voltage is applied to the gate.

13. With regard to Claim 7, Su et al. in view of Zunino teaches the circuit of Claim 5. Zunino further discloses that the second transistor (34) is a p-channel transistor (column 3 lines 38 & 39). A p-channel transistor inherently comprises a channel formed in the p-type substrate beneath the gate region of the transistor when a voltage is applied to the gate.

14. With regard to Claim 8, Su et al. in view of Zunino, discloses an integrated circuit of ESD protecting as described above. The integrated circuit taught by Su et al. in view

of Zunino discloses a silicon-controlled rectifier, a p-type transistor (Zunino Figure 3, 34) formed integrally with the SCR, an n-type transistor (Zunino Figure 3, 16) formed integrally with the SCR, and a control circuit coupled to the to the p-type and n-type transistors.

Zunino further teaches that the integrated circuit is operated at a first DC holding voltage, and a second, lower, DC holding voltage. Su et al. also discloses that the SCR is operated at two different DC voltages to trigger the SCR.

15. With regard to Claim 9, Su et al. in view of Zunino teaches the circuit of Claim 8. Su et al. further discloses that the control circuit comprises a resistor and a capacitor. The circuit taught by Su et al. in view of Zunino teaches that the output terminal (106) is disposed between the resistor and capacitor.

16. With regard to Claim 10, Su et al. in view of Zunino discloses the circuit of Claim 8. Zunino, in Figure 3, further discloses that the gates of the p-type and n-type transistors (34 & 16) are coupled to an output terminal (106).

17. With regard to Claim 11, Su et al. in view of Zunino discloses the circuit of Claim 8. Zunino, in Figure 3 further discloses that the SCR comprises a p-type substrate (18b) an n-well (11'a) formed in the p-type substrate, a p-type diffused region (35) formed in the n-well and an n-type diffused region (22) formed outside of the n-well.

18. With regard to Claim 12, Su et al. in view of Zunino teaches the circuit of Claim 11. Zunino further discloses that the SCR further comprises a p-type diffused region serving as the source of the p-type transistor. Zunino also discloses a different p-type diffused region partially formed in the n-well. Figure 3 discloses that the drain of p-channel transistor (34) is coupled to the source of n-type transistor (16). This requires that either the p-type diffusion reasons 36 and 26 form one solid well, or that aluminum film 48 and 28 are one physical piece. Figure 3 thus teaches that the p-type diffused region partially formed in the n-well serves as the drain of the p-type transistor.

19. With regard to Claim 13, Su et al. in view of Zunino teaches the circuit of Claim 11. Zunino further teaches that the n-type diffused region (22) serves as the source of the n-type transistor. Zunino further discloses that the SCR further comprises a different n-type diffused region (20) formed in the p-substrate to serve as a drain of the n-type transistor (16).

20. With regard to Claim 14, Su et al. in view of Zunino teaches the circuit of Claim 8. Su et al. in figure 4, further discloses that the SCR is coupled between a contact pad (204) and a voltage line (226).

21. With regard to Claim 15, Su et al. in view of Zunino discloses the circuit of Claim 8. Zunino, in Figure 3, further discloses that the SCR, comprised of two MOS transistors (16 & 34) is coupled between different voltage lines (82 & 84).

22. With regard to Claim 23, Su et al. in view of Zunino teaches a method of electrostatic discharge as described above. Su et al. in view of Zunino teaches that the method provides a silicon-controlled rectifier (SCR) (Zunino Figure 1) having a holding voltage; integrally forming a first transistor (34) of a first type with the SCR including a first gate (42); integrally forming a second transistor (16) of a second type with the SCR including a second gate (24); and providing a first signal to the first and second gates to raise the holding voltage of the SCR to keep the SCR from latching up; and providing a second signal to the first and second gates to lower the holding voltage of the SCR to keep the SCR in the latch-up state (Su et al. column 4 lines 42-58).

23. With regard to Claim 24, Su et al. in view of Zunino discloses the method of Claim 23. Su et al. further discloses RC circuitry formed by a resistor (216) and a capacitor 218 that provides a high level signal to the gate of an NMOS transistor (220) to turn on the transistor. As a result, the control circuit (222) exhibits a smaller resistance than the substrate resistance of the SCR (200) (column 4 lines 42-58). The applicant teaches that this raises the holding voltage of the SCR (200), to a value above the power supply voltage.

24. With regard to Claim 25, Su et al. in view of Zunino, the method of Claim 23. Su et al. further discloses that lowering the holding voltage when an ESD occurs by turning

the MOSFET (220) off. Su et al. teaches that without this transistor, the holding voltage is decreased to a minimum holding voltage (column 2 14-23).

25. With regard to Claim 26, Su et al. in view of Zunino discloses the method of Claim 23. Su et al. further discloses that an SCR is coupled between a contact pad (204) and a voltage line (226).

26. With regard to Claim 27, Su et al. in view of Zunino discloses the method of Claim 23. Zunino, in Figure 3, further discloses coupling the SCR (34 & 16) between different voltage lines (82 & 84).

27. Claims 16-22 & 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Su et al. (US 6590261) in view of Zunino (US 4646124) and further in view of Tong et al. (US 6756834).

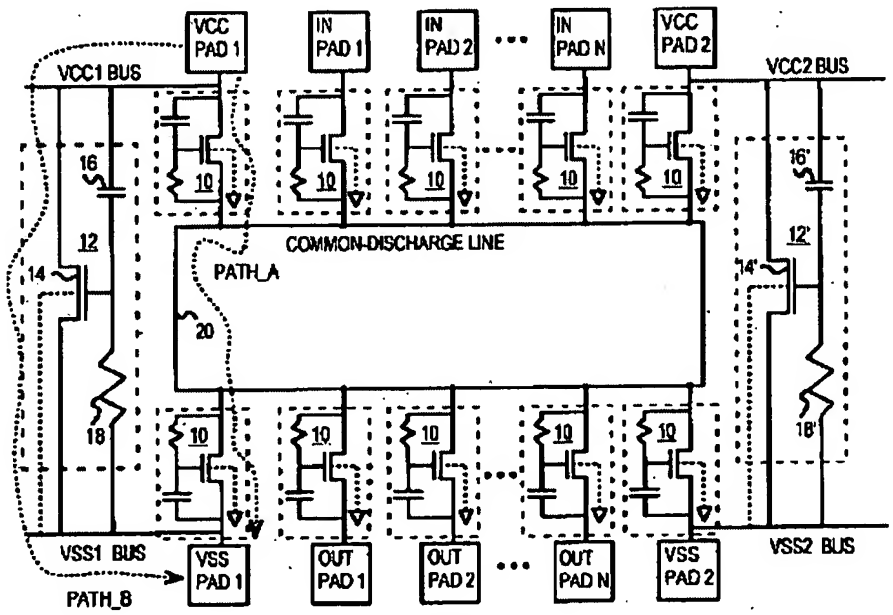


FIG. 1

28. With regard to Claims 16 & 28 Su et al. in view of Zunino discloses an integrated circuit and a method for electrostatic discharge protection as described above. The circuit comprises a first voltage line of a first voltage level (Zunino Figure 3, 82), a second voltage line of a second voltage level (Zunino Figure 3, 84) and a plurality of contact pads (Zunino Figure 3, 82, 84, & 106). Su et al. in view of Zunino further discloses an SCR including a p-type transistor and an n-type transistor integrally formed with the SCR and a control circuit providing a first holding voltage through the p-type and n-type transistors and providing a second holding voltage as described above.

Su et al. in view of Zunino does not disclose that the safety circuit comprises a plurality of silicon-controlled rectifiers.

Tong et al., in figure 1, discloses an ESD protection circuit comprising a plurality of pads, first and second voltage sources of first and second voltage levels, and a plurality of ESD protection circuits (10 & 14). Tong et al. further teaches that each ESD protection device contains a control circuit comprising a capacitor (16) and a resistor (18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Su et al. in view of Zunino with Tong et al. by protecting a plurality of I/O pads and voltage lines with the SCR device taught by Su et al. in view of Zunino for the purpose of providing ESD protection to an entire chip assembly instead of just a single I/O pad.

29. With regard to Claim 17 & 29, Su et al. in view of Zunino and further in view of Tong et al. discloses the circuit of Claim 16 and the method of Claim 28. Tong et al. further discloses that an ESD device (14) is coupled between the first and second voltage lines (VCC & VSS) and that the remaining ESDs are each coupled between a corresponding contact pad and the second voltage line.

30. With regard to Claim 18 & 30, Su et al. in view of Zunino and further in view of Tong et al. discloses the circuit of Claim 17 and the method of Claim 29. Tong et al. further discloses, in Figure 1, that the ESD pulse is discharged from one of the contact pads (VCC PAD 1) via a voltage line (VCC1) to voltage line (VSS 1). This event is depicted by PATH_B in Figure 1.

31. With regard to Claims 19 & 31 Su et al. in view of Zunino and further in view of Tong et al. discloses the circuit of Claim 17 and the method of Claim 29. Tong et al., in Figure 1, further discloses that an ESD pulse is discharged from the first voltage (VCC 1) line via the second voltage (20) line to one of the contact pads (VSS PAD 1) via PATH_A.

32. With regard to Claim 20 & 32, Su et al. in view of Zunino and further in view of Tong et al. discloses the circuit of Claim 17 and the method of Claim 29. Tong et al., in Figure 1, further discloses that an ESD pulse is discharged from one of the contact pads

(VCC PAD 1) via the second voltage line (20) to a different contact pad (VSS PAD 1) via PATH_A.

33. With regard to Claim 21, Su et al. in view of Zunino and further in view of Tong et al. discloses the circuit of Claim 16. Tong et al. further discloses that the control circuit comprises a resistor-capacitor delay circuit.

34. With regard to Claim 22, Su et al. in view of Zunino and further in view of Tong et al. discloses the circuit of Claim 16. Zunino further discloses that the gates of the p-type and n-type transistors are coupled to an output terminal (106). In the ESD protection circuit taught by Su et al. in view of Zunino and further in view of Tong et al., the circuit comprises a plurality of ESD protection circuits arranged in a configuration taught by Tong et al. Each control circuit of the ESD protection devices comprises an output terminal (106) coupled to a gate of each of the p-type (34) and n-type (16) transistors formed in the PNPN transistor taught by Zunino.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB

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